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PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	James C. McKinnell	Confirmation No.:	5091
Application No.:	10/029,649	Examiner:	
Filing Date:	12/20/2001	Group Art Unit:	2814

Title: Substrates Bonded with Oxide Affinity Agent and Bonding Method

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
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TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 10/14/2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

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Rev 10/05 (ApiBrief)

PATENT APPLICATION
Docket No. HP3-061US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	McKinnell, James	)
Serial No.:	10/029,649	) Appeal No.
Confirmation No.	5091	)
Filed:	September 6, 2001	)
For:	Silicide Bond with Integral Surface Getter	)
Examiner:	Mai, Anh D.	)

The Honorable Commissioner of Patents
Mail Stop Appeal Brief - Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

BRIEF OF APPELLANT

The Appellant has filed a timely Notice of Appeal from the action of the Examiner in finally rejecting all of the claims that were considered in this application. This Brief is being filed under the provisions of 37 C.F.R. § 1.192. The Filing Fee, as set forth in 37 C.F.R. § 1.17(c), is submitted herewith.

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Company, by way of assignment from James McKinnell, who is sole named inventor and is captioned in the present brief.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Allowed Claims: No claims have been allowed.

Withdrawn Claims: Claims 18-32, and 35-59 were withdrawn in response to restriction requirement dated March 29, 2004.

Cancelled Claims: Claims 5, 12 and 13 were previously cancelled.

Pending Claims: Claims 1-4, 6-11, 14-17 and 33-34 are pending in the application and stand finally rejected by the Examiner.

Appealed Claims: All of the pending claims are subject to this appeal.

STATUS OF AMENDMENTS

A Final Office Action was issued on June 20, 2005 whereupon Appellant filed a Response on July 27, 2005 to address the 35 U.S.C. §103 rejections of pending claims 1-4, 6-11, 14-17, 33 and 34 and requested reconsideration. No claims were amended in the Response.

An Advisory Action was issued on August 11, 2005 responding to the Appellant's request for reconsideration and maintaining the rejection of the pending claims 1-4, 6-11, 14-17, 33 and 34.

Appellant filed a Notice of Appeal on October 14, 2005 in response to the Advisory Action and the Final Office Action.

SUMMARY OF INVENTION

Beginning at page 6 of the subject Application, devices are described having a bonding structure including an alloy composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and a first substrate.

For example, pages 6-7 beginning at paragraph [0024] describe a device having a bonding material with a reducing agent dispersed therein which is capable of removing oxidation on surfaces to be bonded together such that the oxidation can be removed during the bonding process. When a native oxide is formed upon a surface that is to be joined to another surface, it is desirable to remove the native oxide in order to form a strong and uniform bond to the other surface. By dispersing a reducing agent in a bonding material and then placing the bonding material in contact with the native oxide in a bonding process, the native oxide will be removed. The removal of the native oxide occurs because the agent has a higher affinity for oxygen than the underlying material upon which the native oxide has formed. The agent in the bonding material greatly increases the driving force for the removal of the native oxide, thus enabling a uniform bond between surfaces to be joined together. As the bonding process proceeds at an elevated temperature, the oxygen in the native oxide

will diffuse into the bulk of the bonding material. With the agent dispersed in the bonding material, the oxygen will preferentially combine with the agent so as to remove the native oxide at an increased rate.

Following is a brief summary of independent claims 1, 10, 15, and 33 with exemplary references to the disclosure inserted for convenience. References should not be understood as limiting any feature to the recited portions of the disclosure.

Independent Claim 1 recites an electrical device (e.g., FIG. 4, 200, p.11) comprising "first and second substrates (e.g., FIG.4, 104,102) having respective first and second integrated circuits" (e.g. FIG. 1, 110, p. 7), wherein "at least one of the first substrate or the second substrate has a semiconductor layer (e.g., FIG.4 126, p. 11) thereon"; and "a bond structure (e.g., FIG. 2, 114 p. 10-11) bonding the first substrate to the second substrate, the bond structure including an alloy", "bonded to the semiconductor layer;" "composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate;" (e.g., FIG. 4, 124, p.6-7, p.10-11) and "configured to form an electrical connection between the first integrated circuit and the second integrated circuit." (e.g., FIG. 4, p. 8)

Independent Claim 10 recites an electrical device (e.g., FIG. 4, 200, p.11) comprising "first and second semiconductor wafers (e.g., FIG.4, 104,102) each including a plurality of integrated circuits" (e.g. FIG. 1, 110, p. 7), wherein "the first semiconductor wafer has a silicon layer thereon" (e.g., FIG.4 126, p. 11), "the silicon layer on the first semiconductor wafer is bonded to the second semiconductor wafer by gold alloyed (e.g., p. 9) with an oxide affinity material having an oxygen affinity higher than that of silicon such that the gold alloyed with the oxide affinity material is sufficient to remove a native oxide from the first semiconductor wafer" (e.g., FIG. 4, 124, p.6-7, p.10-11) and "the gold alloyed with the oxide affinity material is configured to provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer" (e.g., FIG. 4, p. 8).

Independent Claim 15 recites an electrical device (e.g., FIG. 4, 200, p.11) comprising "first and second semiconductor wafers each including a plurality of integrated circuits" (e.g. FIG. 1, 110, p. 7), "silicon on the first semiconductor wafer" (e.g., FIG.4 126, p. 11) and "a bonding structure (e.g., FIG. 2, 114 p. 10-11) including gold alloyed (e.g., p. 9) with a material having a free energy lower than that of silicon dioxide" wherein "the first semiconductor wafer is bonded to the second semiconductor wafer by the gold alloy that is bonded to the silicon on the first semiconductor wafer" such that "the gold alloy is configured to: remove a native

oxide from the silicon;" (e.g., FIG. 4, 124, p.6-7, p.10-11) and "provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer" (e.g., FIG. 4, p. 8).

Independent Claim 33 recites an electrical device (e.g., FIG. 4, 200, p.11) comprising "first and second substrates bonded together (e.g., FIG.4, 104,102) with a first material having dispersed therein a reducing agent for the diffusion therein of oxidation of a second material of which at least one of the first and second substrates is composed' wherein " the reducing agent has a higher affinity for oxygen than that of the second material " and "the first material having the dispersed reducing agent is configured to: remove a native oxide from the first substrate or the second substrate; (e.g., FIG. 4, 124, p.6-7, p.10-11) and form an electrical connection between a first integrated circuit on the first substrate with a second integrated circuit on the second substrate" (e.g., FIG. 4, p. 8).

GROUNDS OF REJECTION

1. Whether claims 1, 3-4, 6-10, 12, 14-16, 33 and 34 were properly rejected under 35 U.S.C. § 103(b) as being obvious over U.S. Patent No. 6,118,181 to Merchant et. al (hereinafter "Merchant") in view of by U.S. Patent No. 5,702,962 to Terasawa (hereinafter "Tersasawa").

2. Whether claims 2, 11, and 17 were properly rejected under 35 U.S.C. § 103(b) as being obvious over Merchant in view of Terasawa in further view of U.S. Patent No. 5,668,033 to O'Hara et al. (hereinafter "Ohara").

ARGUMENT

FIRST GROUND OF REJECTION: Claims 1, 3-4, 6-10, 12, 14-16, 33 and 34 satisfy the requirements of 35 U.S.C. § 103(a) and therefore are patentable over the proposed combination of Merchant and Terasawa.

1. Summary of the References

Merchant describes a system and method for bonding wafers. Although Merchant describes integrated circuits on two wafers, Merchant recites that "most conventional wafer bonding processes are not suitable for bonding wafers that include CMOS circuitry and other temperature sensitive components because the relatively high temperatures associated with the bonding process can damage the CMOS circuitry or other temperature sensitive components." *See Merchant, Col. 1, Lines 34-39.* Merchant then describes an instance of such an undesirable and unacceptable bonding technique in the following excerpted portion:

> In addition, it is often undesirable to use eutectic bonding in order to bond two wafers together because the existence of liquid phases in these processes can sometimes lead to rapid dissolution of underlayers and, hence, a loss of process control. Furthermore, maintaining precise separation distances between two wafers bonded via eutectic bonding can be difficult since the surfaces of the eutectics typically deform when a temperature close to the eutectic's melting point is reached. *Merchant, Col. 1, Lines 52-62.*

Consequently, Merchant describes a bonding process that uses palladium in response to the undesirability of eutectic bonding. Merchant also cautions that "one skilled in the art should realize that substituting for the silicon and/or palladium may affect the temperatures associated with the bonding process". *See Merchant, Col 6, Lines 24-23 and 17-19.* Therefore, Merchant explicitly cautions against the use of materials other than palladium and

against the use of eutectic bonding.

Further, Merchant describes the following:

> It should be further noted that the adhesion of palladium to chromium has been found to depend directly on the cleanliness of the chromium layer 29 surface. Therefore, it is preferable to perform a brief (i.e., approximately 1 to 2 minutes) 150 W rf sputter-etch cleaning of the chromium layer 29 surface just prior to application of the palladium layer 27 to the chromium layer 29. *Merchant, Col. 4, Lines 31-37.*

Thus, Merchant discloses sputter-etch cleaning of the chromium layer before adhesion of the palladium. Nowhere does Merchant disclose, teach or suggest a bond structure having an alloy that is sufficient to remove a native oxide.

Terasawa describes a fabrication process for a static induction transistor. In the fabrication process of Terasawa, an oxide film is removed with hydrofluoric acid, as shown in the following excerpt:

> The naturally formed oxide film is then removed with hydrofluoric acid as needed, and the N.sup.- substrate 10 and the N.sup.+ substrate 20 are subjected to ultrasonic cleaning with purified water and dried by a spin dryer at room temperature *Terasawa, Col. 4, Lines 47-50.*

To clean the surfaces, Terasawa describes the following:

> The N.sup.- substrate 10 and the N.sup.+ substrate 20 are then subjected to ultrasonic cleaning with an aqueous solution of sulfuric acid and hydrogen peroxide, thereby removing organic substances and metals on the substrates. *Terasawa, Col. 9, Lines 13-16.*

Thus, Terasawa discloses the use of acids to remove oxide films and clean surfaces. Nowhere does Terasawa disclose, teach or suggest a bond structure having an alloy that is sufficient to remove a native oxide.

2. **The proposed combination of Merchant and Terasawa fails to teach or suggest all recited features as required to establish a prima facie case of obviousness.**

It is well settled that, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); *MPEP § 2142*. The proposed combination of Merchant and Terasawa fails to teach or suggest all the features of the Appellant's claimed invention. To simplify the following discussion, independent Claim 1 will be discussed as an example with the reasoning being equally applicable to independent claims 10, 15 and 33.

Independent **Claim 1** recites "a bond structure ... including an alloy ... composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed ***such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate***". (emphasis added). The Examiner asserts that "there are no native oxide existed between the bond structure and the first and second substrates of Terasawa '962 and Merchant '181, therefore, the claimed term is met". *Office Action Dated June 15, 2005, Page 4*. The Appellant respectfully and strongly disagrees. Respectfully, the proposed combination of Merchant and Terasawa fails to teach or suggest "a bond structure ...including an alloy ... composed of noble metal alloyed with an oxide affinity material ...such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate" as recited in Claim 1.

As shown in the above excerpts, Merchant describes "a brief (i.e., approximately 1 to 2 minutes) 150 W rf sputter-etch cleaning of the chromium layer 29 surface just prior to

application of the palladium layer 27 to the chromium layer 29". *Merchant, Col. 4, Lines 31-37.* Terasawa describes "ultrasonic cleaning with an aqueous solution of sulfuric acid and hydrogen peroxide, thereby removing organic substances and metals on the substrates". *Terasawa, Col. 9, Lines 13-16.* This is required in both these references, alone and in combination, to form the bond structure because "adhesion of palladium to chromium has been found to depend directly on the cleanliness of the chromium layer 29 surface". *Merchant, Col. 4, Lines 31-33.* Thus, both Merchant and Terasawa teach a bond structure that requires separate cleaning of the substrates before application.

Thus, neither of the bond structures of Merchant nor Terasawa teach or suggest the recited bond structure of Claim 1 having an alloy that includes "an oxide affinity material ... such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate". By including such an oxide affinity material **in the amount recited**, cleaning of the oxide is not required as is specifically recited by each of the references asserted by the Examiner. Thus, there is no teaching or suggestion in either of the references for such a feature, alone or in combination, because, as stated by the references and by the Examiner, other cleaning techniques are utilized to remove an oxide film. In fact, as described in detail under point 3 below, the Examiner has not indicated a teaching or suggestion in the references, alone or in combination, but rather has chosen to ignore this recited feature. Accordingly, the combination of Merchant and Terasawa fails to teach or suggest all the recited features of Claim 1 and a prima facie case of obviousness has not been established.

3. **The Examiner has improperly ignored recited features of the claims and mischaracterized the claims as product by process claims.**

The Examiner has failed to indicate where either of the references, alone or in

combination, teach or suggest the recited alloy of Claim 1, but rather has ignored the recited features (e.g., "given no patentable weight"), which is described in greater detail below. For example, Examiner argues:

> "Applicant asserts that Merchant does not teach or suggest a bond structure having an alloy this is sufficient to remove a antive oxide. As previously discussed, Applicant argues interm of process while the claims are clearly directed to a semiconductor device. As a devicc there is no oxide at the interface of the bonding structure. Therefore, the argument regarding whether or not the oxide existed prior to the bonding process is irrelevant". *Advisory Action dated 8/11/2005 Continuation Sheet.*

Appellant strongly disagrees. It is respectfully submitted that the Examiner has mischaracterized the features of Claim 1. As described in detail below, the recited feature at issue describes an amount of oxide affinity material that is included in the alloy and does not recite a process for making the alloy. Respectfully, the Examiner improperly determines that the recited feature is irrelevant and ignores the recited feature.

The Examiner asserts that the "expression 'such that the gold the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate' is/are taken to be a product by process limitation and is given no patentable weight". *Office Action Dated June 15, 2005, Page 4.* Again, it is respectfully submitted that the Examiner has mischaracterized the features of Claim 1. For example, in the "Training Materials for Treatment of Product and Process Claims in Light of *In re Brouwer* and *In re Ochiai* and 35 U.S.C. 103(b)", the Office provides guidance regarding distinctions between product claims and product by process claims. The referenced training materials are

available at http://www.uspto.gov/web/offices/pac/dapp/ppclms.htm. For example, in the following section, product and process claims are discussed, respectively:

> Claim 1. A p-n junction device comprising:
>
> a substrate composed of a semiconductor material;
>
> a heavily doped n-type subcollector layer over said substrate;
>
> a n-type collector layer over said subcollector layer;
>
> a heavily doped p-type first base layer over said collector layer;
>
> a p-type second base layer over said first base layer; and
>
> a n-type emitter layer over said second base layer, whereby said second base layer serves as a diffusion barrier between said base and said emitter.
>
> Claim 2. A method of forming heterojunction device comprising the steps of:
>
> forming a heavily doped n-type subcollector layer over a semiconductor substrate;
>
> forming an n-type collector layer over said subcollector layer;
>
> forming a heavily doped p-type first base layer over said collector layer;
>
> forming a p-type second base layer over said first base layer; and
>
> forming an n-type emitter layer over said second base layer, whereby said p-type second base layer serves as a diffusion barrier between said p-type first base layer and said n-type emitter layer.
>
> *See Training Materials for Treatment of Product and Process Claims in Light of In re Brouwer and In re Ochiai and 35 U.S.C. 103(b).*

As recited in the training materials, Claim 1 in the above example is drawn to a product and Claim 2 is drawn to a process (e.g., "the product of claim 1 and process of claim 2"), even though relative amounts of the materials are claimed in claim 1, e.g., "a heavily doped p-type

first base layer". Thus, the recitation of "a bond structure ... composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed ***such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate***" as recited in Appellant's Claim 1 recites an amount of oxide affinity material and is clearly an apparatus claim which includes a recitation of an amount of a material in an element of the apparatus, and not a process step.

As stated by the MPEP, a product by process claim "is a product claim that defines the claim product *in terms of the process by which it is made*". *See MPEP, 2173.05(p (emphasis added)*. For example, Claim 2 taken from the training material above is one such example of a product-by-process claim. In the present case, however, the recited feature describes an amount of oxide affinity material that is included in the alloy and does not recite a process for making the alloy. Clearly, an apparatus claim may recite elements having claimed amounts of material, and that such a recitation does not move the claim to a "product-by-process", but rather claims features of the apparatus itself. Therefore, Claim 1 is not a product by process claim. Accordingly, the Examiner's assertion that "no native oxide existed between the bond structure and the first and second substrates of Terasawa '962 and Merchant '181, therefore, the claimed term is met" is respectfully submitted to be incorrect. *Office Action Dated June 15, 2005, Page 4.*

Even assuming *for the sake of argument alone* that this feature (i.e., the amount) recites a process in a product-by-process claim, the Examiner must still show how "[t]he structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over prior art". *See MPEP 2113.* Therefore, the Examiner is to give the recited feature patentable weight even in the instance of a product-by-process claim

and must show where the structure formed by the process is taught or suggested by the references. Therefore, the Examiner's assertion that "a product by process limitation and is given no patentable weight" does not meet this requirement and is contrary to the express requirements of the MPEP. *Office Action Dated June 15, 2005, Page 4.* Further, it should be noted that absent such a showing, the burden does not shift to the Appellant. *See MPEP 2113.*

In the *Response to Arguments* section, the Examiner asserts that the "product of the claims is 'a bond structure composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed". *See Office Action Dated June 15, 2005, Page 15.* Again, the Examiner makes no mention of the recited feature which claims an amount of the oxide affinity material in the bond structure, i.e., "composed such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate" as recited in Claim 1. As previously stated, neither of the asserted references, alone or in combination, teach nor suggest such a bond structure because each of these references requires cleaning of an oxide before bonding using the bond structure. Therefore, even assuming *for the sake of argument alone* that the burden has shifted to the Appellant to show that the products are different, this burden has also been addressed.

Additionally, in the *Response to Arguments* section, the Examiner asserts that the "limitations of the claim do not recite that oxide exist at the interface of the bonding structure, but 'the alloy is sufficient to remove a native oxide from an interface surface'". *See Office Action Dated June 15, 2005.* Again, it is respectfully submitted that the Examiner has misinterpreted the claim. The recited feature claims an amount and not a process, which becomes apparent when recited as a whole, i.e., "bond structure including an alloy: bonded to

the semiconductor layer; and composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed **such that** the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate" as recited in Claim 1.

4. **There is insufficient motivation for the proposed combination of Merchant and Terasawa as the combination is against the express teachings of the references.**

As previously indicated a *prima facie* case of obviousness requires some suggestion or motivation to modify the reference or to combine reference teachings. These references may not be modified as suggested because such a modification runs contrary to the express teachings of the references as excerpted above.

Both Merchant and Terasawa describe a cleaning step prior to bonding. Merchant describes "a brief (i.e., approximately 1 to 2 minutes) 150 W rf sputter-etch cleaning of the chromium layer 29 surface just prior to application of the palladium layer 27 to the chromium layer 29". *Merchant, Col. 4, Lines 31-37.* Terasawa describes "ultrasonic cleaning with an aqueous solution of sulfuric acid and hydrogen peroxide, thereby removing organic substances and metals on the substrates". *Terasawa, Col. 9, Lines 13-16.* This is required in both these references, alone and in combination, to form the bond structure because "adhesion of palladium to chromium has been found to depend directly on the cleanliness of the chromium layer 29 surface". *Merchant, Col. 4, Lines 31-33.* In other words, combining two references, each of which requires a cleaning, does not produce the claimed invention which includes a bond structure with oxide affinity material sufficient to remove a native oxide nor would one of ordinary skill in the art combine them. Such an amount of oxide affinity material is specifically not taught or suggested because both references, alone or in

combination, require cleaning.

Further, the Examiner acknowledges that Merchant fails to teach "using a bonded structure composed of noble metal alloyed with an oxide affinity material." *Office Action dated June, 15 2005 p. 3.* To correct this defect the Examiner cites Terasawa for a bond structure of gold and antimony (Au-Sb). *Id.* However, Merchant describes a bonding process that uses palladium in response to the undesirability of eutectic bonding. In addition, Merchant also cautions that "one skilled in the art should realize that substituting for the silicon and/or palladium may affect the temperatures associated with the bonding process". *See Merchant, Col 6, Lines 24-23 and 17-19.* Therefore, Merchant explicitly cautions against the use of materials other than palladium and against the use of eutectic bonding. Thus, the proposed combination of the bond structure in Terasawa with Merchant is contrary to the express teachings of Merchant. Accordingly, one of ordinary skill in the art would not make the proposed combination of Merchant with Terasawa.

It is respectfully submitted that a prima facie case of obviousness had not been established. Accordingly, Claim 1 is patentable over Merchant and Terasawa, alone or in combination and reversal of the rejection is respectfully requested. **Claims 3-4 and 6-9** which depend from Claim 1 are patentable at least based upon this dependency and reversal of the rejection is respectfully requested.

5. **Claims 10, 15, and 33 and their respective dependent claims are patentable for at least the reasons discussed with respect to Claim 1**

Claim 10 recites "gold alloyed with an oxide affinity material having an oxygen affinity higher than that of silicon such that the gold alloyed with the oxide affinity material is sufficient to remove a native oxide from the first semiconductor wafer". Claim 10 is

allowable based on similar reasoning as previously recited for Claim 1. As previously described, there is no teaching or suggestion in neither Merchant nor Terasawa, alone or in combination, for the recited feature. Additionally, these references may not be modified because such a modification runs contrary to the express teachings of the references and even the assertions made by the Examiner.

The Examiner also asserts that the "expression 'such that the gold alloyed with the oxide affinity material is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate' is/are taken to be a product by process limitation and is given no patentable weight". *Office Action Dated June 15, 2005, Page 7.* It is respectfully submitted that the Examiner has also mischaracterized the features of Claim 10. The recited feature describes an amount of oxide affinity material included with the gold. The recited feature does not recite a process. As stated by the MPEP, a product by process claim "is a product claim that defines the claim product in terms of the process by which it is made". *See MPEP, 2173.05(p).* In the present case, the recited feature does not recite process for making the alloy, but rather recites a composition of the alloy. Therefore, Claim 10 is not a product by process claim. Thus, the Examiner's assertion that "no native oxide existed between the bond structure and the first and second substrates of Terasawa '962 and Merchant '181, therefore, the claimed term is met" is again respectfully submitted to be incorrect and does not follow the procedure for examination prescribed by the MPEP, e.g., §§ 2113, 2173.05(p). *Office Action Dated June 15, 2005, Page 7.*

Accordingly, for at least these reasons a *prima facie* case of obviousness has not been established with respect to Claim 10 and reversal of the rejection is respectfully requested.

Claims 11 and **14** depend from independent Claim 10. Each of these claims is allowable based on their respective dependencies as well as their own recited features which

are not disclosed, taught, or suggested the references of record, alone or in combination.

Claim 15 recites a "gold alloy is configured to ***remove a native oxide from the silicon***; and provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer". **Claim 33** recites a "first material having the dispersed reducing agent is configured to ***remove a native oxide from the first substrate or the second substrate;*** and form an electrical connection between a first integrated circuit on the first substrate with a second integrated circuit on the second substrate".

Claims 15 and 33 are allowable based on similar reasoning as previously recited for Claims 1 and 10 and therefore the Appellant will not further burden the record by repeating each of the arguments. As previously described, there is no teaching or suggestion in neither Merchant nor Terasawa, alone or in combination, for the recited feature. Additionally, these references may not be modified because such a modification runs contrary to the express teachings of the references and even the assertions made by the Examiner.

Further, the Application again respectfully submits that the Examiner has mischaracterized the features of the claims. The recited features describe an amount of oxide affinity material and do not recite a process. As stated by the MPEP, a product by process claim "is a product claim that defines the claim product in terms of the process by which it is made". *See MPEP, 2173.05(p).* In the present case, the recited feature does not recite a process for making the gold alloy, but rather recites a composition of the alloy. Therefore, Claims 15 and 33 are not a product by process claims.

Accordingly, for at least these reasons a *prima facie* case of obviousness has not been established with respect to Claims 15 and 33 and reversal of the rejection is respectfully requested.

Claim 16 depends from independent Claim 15. **Claim 34** depends from independent Claim 33. Each of these claims is allowable based on their respective dependencies as well as their own recited features which are not disclosed, taught, or suggested the references of record, alone or in combination.

Accordingly, it is respectfully submitted that Claims 1, 3-4, 6-10, 12-16 and 33-34 are allowable over Merchant and Terasawa, alone and in combination. Appellant respectfully requests that the First Ground of Rejection be overturned.

SECOND GROUND OF REJECTION: Claims 2, 11, and 17 satisfy the requirements of 35 U.S.C. § 103(a) and therefore are patentable over the proposed combination of Merchant and Terasawa in further view of OHara.

1. **Claims 2, 11, and 17 are patentable over the proposed combination of Merchant and Terasawa in further view of OHara.**

Reference is made to the previous discussion of **Merchant** and **Teresawa** so as to avoid further burdening of the record. As previously described the combination fails to teach or suggest an alloy that includes "an oxide affinity material ... such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate". Ohara does not correct the defects in the combination of Merchant and Teresawa.

Ohara describes a method for manufacturing a semiconductor acceleration sensor device by "covering a movable portion by use of a cap". *See Ohara, Col. 1, Lines 51-52.* Ohara describes the bonding of the cap as follows:

> Also, preferably, a gold (Au) film is adhered to the leg portion of the cap forming wafer. Where the bonding frame is made to be formed using silicon (Si), when in the bonding step heating is performed up to a temperature higher than an Au/Si eutectic temperature, the gold film comes to function as a bonding layer, with the result that it is possible to obtain a tough bondage easily. Further, when the gold film is also adhered onto the inner surface of the cap, the gold film can be also made to function as an electromagnetic shielding layer. *Ohara, Col. 2, Lines 23-32.*

Thus, Ohara merely describes a cap which is bonded using a gold film. The cap described in Ohara merely serves to protect the movable portion of the semiconductor acceleration sensor. The gold film is utilized as a bond via a eutectic technique and may function as an electromagnetic shield. Nowhere does Ohara disclose, teach or suggest an integrated circuit

in the cap. Thus, Ohara does not cure the defects of Merchant and Terasawa in that Ohara does not teach or suggest an alloy that is sufficient to remove a native oxide.

Claim 2 depends from claim 1. **Claim 11** and **Claim 17** depend from Claim 15. Accordingly, these claims incorporate the features of their respective base claim and are allowable based on there respective dependencies to allowable base claims as addressed in relation to the First Ground of Rejection.

Further, there is not sufficient motivation for the asserted combination of Merchant in view of Terasawa in further view of Ohara. Neither Merchant nor Terasawa disclose, teach or suggest any deficiencies with the recited techniques used to clean and remove oxides. Ohara does not teach or suggest that the described bond is suitable for providing an electrical connection between integrated circuits. Therefore, a person of ordinary skill in the art, when viewing Merchant and Terasawa, would not be motivated to look to Ohara for a bonding technique that is utilized to attach a cap.

For at least these foregoing reasons Claims 2, 10, and 11 are allowable over the proposed combination of Merchant in view of Terasawa in further view of Ohara. Accordingly, Appellant respectfully requests that the Second Ground of Rejection be overturned.

CONCLUSION

The Appellant respectfully considers this application to be in condition for allowance and respectfully requests the Board to overturn the final rejection and that the Examiner pass this application to allowance.

Dated this 7th day of Dec, 2005.

Respectfully submitted,

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CLAIMS APPENDIX

1. An electrical device comprising:

first and second substrates having respective first and second integrated circuits, wherein at least one of the first substrate or the second substrate has a semiconductor layer thereon; and

a bond structure bonding the first substrate to the second substrate, the bond structure including an alloy:

bonded to the semiconductor layer;

composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate; and

configured to form an electrical connection between the first integrated circuit and the second integrated circuit.

2. The electrical device as defined in Claim 1, wherein the oxide affinity material is not more than about half the weight of the alloy interfacing the semiconductor layer.

3. The electrical device as defined in Claim 1, further comprising electrical insulation, situated between the first and second substrates electrical insulation, for electrically isolating a plurality integrated circuits.

4. The electrical device as defined in Claim 1, further comprising a region having a closed environment between the first and second substrates, wherein the region is defined at least in part by the bond structure.

6. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is sufficient to maintain an alignment of said first substrate with respect to the second substrate.

7. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with an oxide affinity material having a free energy that is lower than that of silicon dioxide.

8. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with a material having a free energy less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

9. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with a material selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

10. An electrical device comprising first and second semiconductor wafers each including a plurality of integrated circuits, wherein:

the first semiconductor wafer has a silicon layer thereon;

the silicon layer on the first semiconductor wafer is bonded to the second semiconductor wafer by gold alloyed with an oxide affinity material having an oxygen affinity higher than that of silicon such that the gold alloyed with the oxide affinity material is sufficient to remove a native oxide from the first semiconductor wafer; and

the gold alloyed with the oxide affinity material is configured to provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer.

11. The electrical device as defined in Claim 10, wherein the oxide affinity material makes up not more than about half the weight of the gold.

14. The electrical device as defined in Claim 10, further comprising a hermetically sealed region between the first and second semiconductor wafers that is defined in part by:

the silicon layer on the first semiconductor wafer; and

the gold alloyed with the oxide affinity material.

15. An electrical device comprising:

first and second semiconductor wafers each including a plurality of integrated circuits;

silicon on the first semiconductor wafer; and

a bonding structure including gold alloyed with a material having a free energy lower than that of silicon dioxide, wherein the first semiconductor wafer is bonded to the second semiconductor wafer by the gold alloy that is bonded to the silicon on the first semiconductor wafer such that the gold alloy is configured to:

remove a native oxide from the silicon; and

provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer.

16. The electrical device as defined in Claim 15, wherein the free energy of the material is less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

17. The electrical device as defined in Claim 15, wherein the material selected from the group consisting of Ti Al, Li, Mg, and Ca.

33. An electrical device comprising first and second substrates bonded together with a first material having dispersed therein a reducing agent for the diffusion therein of oxidation of a second material of which at least one of the first and second substrates is composed, wherein:

the reducing agent has a higher affinity for oxygen than that of the second material; and

the first material having the dispersed reducing agent is configured to:

remove a native oxide from the first substrate or the second substrate; and

form an electrical connection between a first integrated circuit on the first substrate with a second integrated circuit on the second substrate.

34. The electrical device as defined in Claim 33, wherein:

the first material comprises gold; and

the second material comprises silicon.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.